IN THE SPECIFICATION

Please replace the second paragraph on page 8 with the following paragraph:

Figure 2 is a illustration of a high speed serial memory interface system 200, one embodiment of the present invention. High speed serial memory interface system 200 comprises an information configuration core for coordinating proper alignment of information communication signals, a system interface for communicating with a system controller (not shown) and a memory array interface for communicating with a memory array. In one embodiment of the present invention a system interface comprises 12 serial read data ports for communicating serial read information from a system controller, 12 serial write data ports for communicating serial write information from a system controller, and 3 serial address data ports for communicating serial address information from a system controller. In one embodiment of the present invention, a memory array interface comprises 48 parallel transmit ports for transmitting information to a memory array, 48 parallel receive ports for communicating for receiving information from a memory array, 20 parallel address ports for communicating address information to an address array and 4 control ports for communicating control information to an information array. In the illustrated embodiment there are 12 parallel transmits ports and receive ports each data bits 0-7, 8-15,16-23, 24 -31, 32-39 and 40 -47 and there are 3 address ports for address bits 0-7, 8-15, 16-19 and control bits 0-3. The data ports are clocked at double data rate (500MB/s), while the address and control lines are clocked at 250 MB/s.